HYDRA: a multi-core RISC-V with cryptographically useful modes of operation

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Motivation

- Computing parallelism:
  - Data Level (DLP), Instruction Level (ILP), Thread Level (TLP)
  - DLP via Single Instruction Multiple Data (SIMD) extension
  - The trend from single- toward multi-core processor designs [5]
- Composable lightweight processor [13]
  - Flexible multi-core configuration.
  - Exploit the advantages of DLP and TLP.
- Case study in Cryptography:
  - Performance (i.e., speed up cryptographic software)
  - Security/Reliability (i.e., Fault Attack/Detection).
- The implementation is available: https://github.com/scarv/hydra, under an open-source license

Composable System Design Concept

- Consider a set of p atomic processor cores:

$$P = \{P_0, P_1, \ldots, P_{p-1}\}$$

- Define a composable configuration:

$$C^M(P) = \{\{\overline{P_0}, \ldots, P_{n-1}\}, \{P_n\}, \ldots, \{P_{p-1}\}\}.$$

- The system will be reconfigured as
  - A single n-composed system operating in M mode.

    $C(P)_0^M = \{\overline{P_0}, \ldots, P_{n-1}\}$; $\overline{P_0}$ denotes primary core
  - Multiple single conventional cores

    $C(P)_1 = \{P_n\}; \quad \ldots; \quad C(P)_{p-n} = \{P_{p-1}\}$

- Generic composable computing concept
  - Given two $n \times b$-bit operands represented by b-bit elements:

$$x = \{x_{n-1} \parallel x_{\ldots} \parallel x_0\}; \qquad y = \{y_{n-1} \parallel y_{\ldots} \parallel y_0\};$$

  - And each b-bit processor, p_i, supports $\mathfrak{I}_{\oslash}$ instruction; s_i denotes status flags.

$$\{s_i, r_i\} \leftarrow \mathfrak{I}_{\oslash}^{s_i}(x_i, y_i)$$

  - Compute $\oslash$ operation:

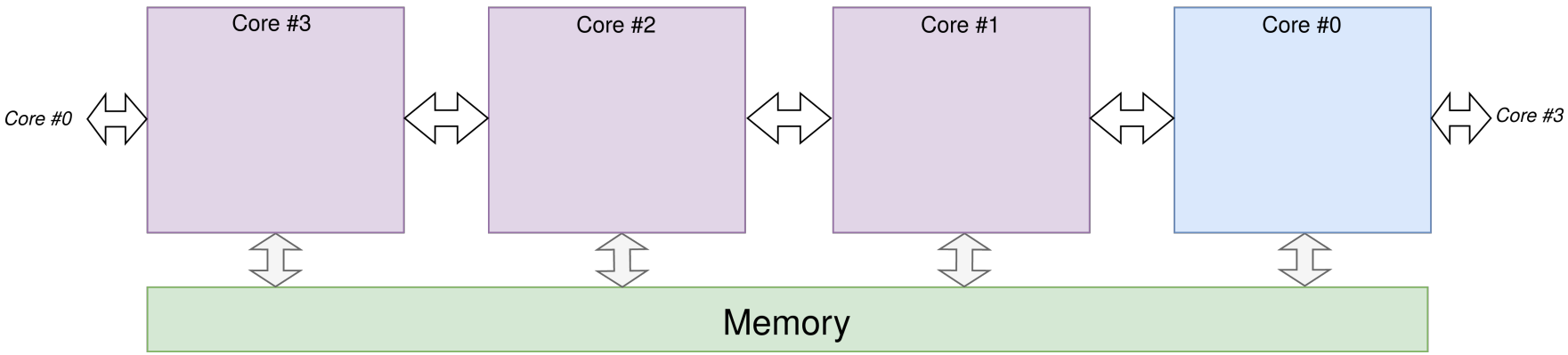
$$r = \{r_{n-1} \parallel r_{\ldots} \parallel r_0\} = x \oslash y = \{x_{n-1} \parallel x_{\ldots} \parallel x_0\} \oslash \{y_{n-1} \parallel y_{\ldots} \parallel y_0\};$$

  - needs:

$$\mathfrak{I}_{\oslash}^{s_0}(x_0, y_0) \longleftrightarrow \mathfrak{I}_{\oslash}^{s_1}(x_1, y_1) \ldots \longleftrightarrow \mathfrak{I}_{\oslash}^{s_{n-1}}(x_{n-1}, y_{n-1})$$

- Three composed modes depend on operation, $\oslash$, and operands (i.e., $\parallel$)

  SIMD Compute Mode, Wide Data-path Mode and SIMD Redundant Mode:



SIMD Compute Mode

- Consider operands are sets of n b-bit elements,
  $\|$: independent elements, denoted $\{\ ;\ \}$

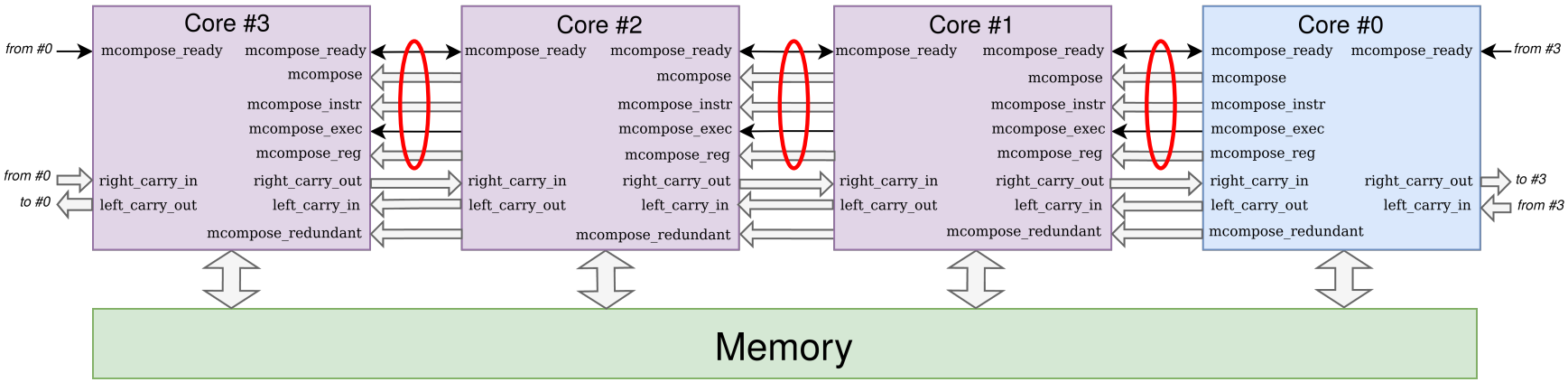
$$x = \{x_{n-1};\ x_{...};\ x_0\}; \qquad y = \{y_{n-1};\ y_{...};\ y_0\};$$

- To compute $\oslash$ operation:

$$r = \{r_{n-1};\ r_{...};\ r_0\} = \{x_{n-1};\ x_{...};\ x_0\} \oslash \{y_{n-1};\ y_{...};\ y_0\};$$

- Each p_i atomic processor core in the composed system.

$$r_i \leftarrow \Im_{\oslash}(x_i, y_i)$$



Wide Data-path Mode

- Consider operands are $n \times b$-bit values,
  $\|$: bit-order dependent elements, denoted { _ }

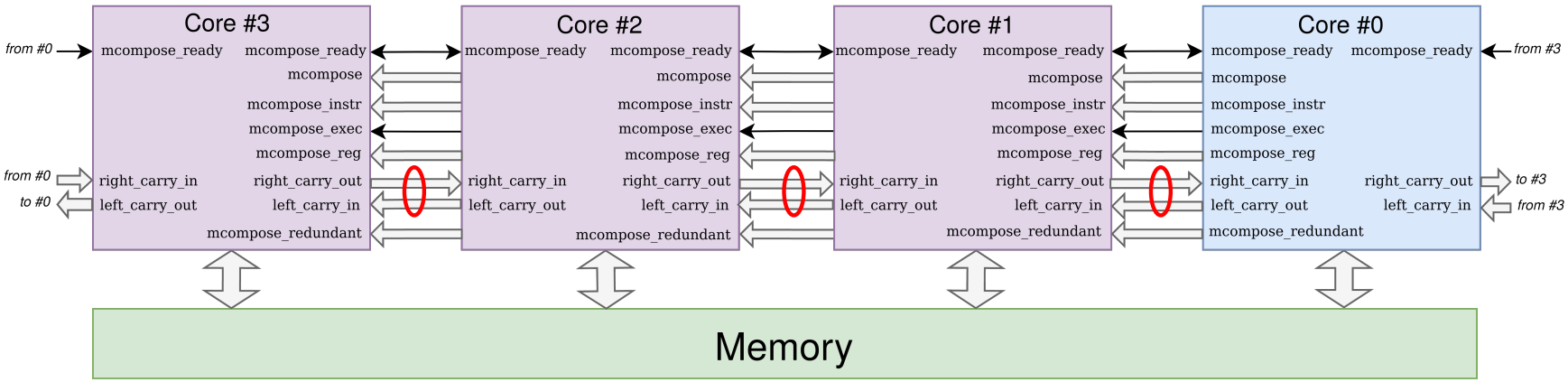
$$x = \{x_{n-1}\_x_{\ldots}\_x_0\}; \qquad y = \{y_{n-1}\_y_{\ldots}\_y_0\};$$

- To compute $\oslash$ operation:

$$r = \{r_{n-1}\_r_{\ldots}\_r_0\} = \{x_{n-1}\_x_{\ldots}\_x_0\} \oslash \{y_{n-1}\_y_{\ldots}\_y_0\};$$

- Each p_i atomic processor core in the composed system.
  $s_i \equiv c_i$: using carrier flags

$$\{c_i, r_i\} \leftarrow \mathfrak{I}_{\oslash}^{c_{i-1}}(x_i, y_i)$$



SIMD Redundant Mode

- Detect if a fault happens on: $\underline{x} \oslash \underline{y}$
- Redundantly extend scalar operands to sets of n same value elements,

$$x = \{\underline{x};\ \ldots;\ \underline{x}\}; \qquad y = \{\underline{y};\ \ldots;\ \underline{y}\};$$

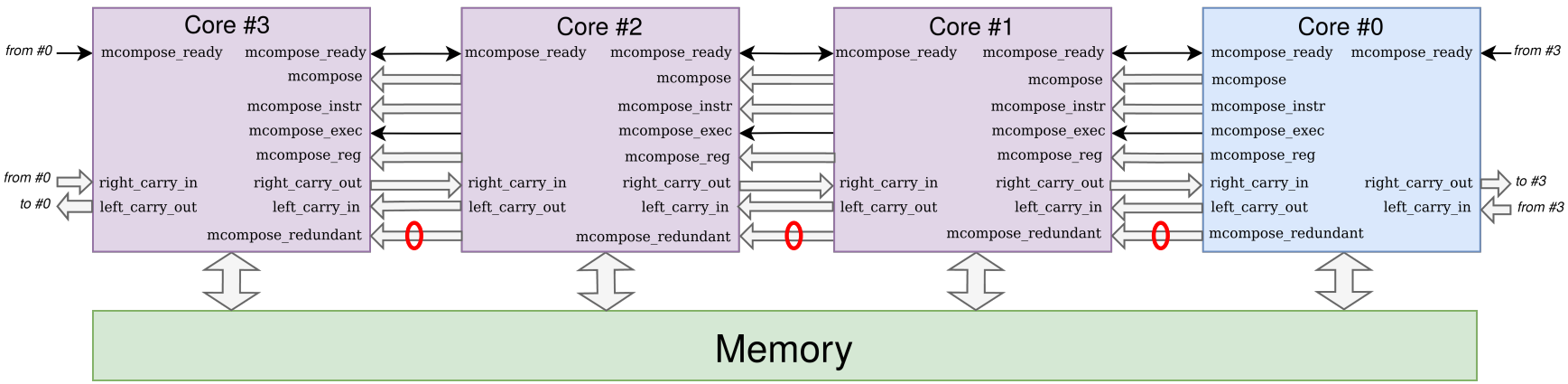
  { ; }: independent elements

- Synchronise : $s_0, s_1, \ldots, s_{n-1}$; Compute $\oslash$: $r = x \oslash y$;
- Each p_i atomic processor core in the composed system.

$$r_i \leftarrow \mathfrak{I}_{\oslash}(x_i, y_i)$$

- To detect a fault, check:

$$\mathfrak{I}_{\oslash}^{s_0}(x_0, y_0) == \mathfrak{I}_{\oslash}^{s_1}(x_1, y_1) \ldots == \mathfrak{I}_{\oslash}^{s_{n-1}}(x_{n-1}, y_{n-1})$$



Hardware Implementation

- A proof of concept on an FPGA platform:
  - Modified PicoRV32[1]: an area-optimised, non-pipelined core
  - Interconnection to connect 4 cores to a shared memory
  - Xilinx Kintex-7 (xc7k160tfbg676) FPGA on SASEBO-GIII [8]
  - Clock speed of 50 MHz
- Hardware overheads of 4-core conventional v.s. composable alternative

	LUTs	FFs	Longest delay	
Original core	1425 (1.00×)	968 (1.00×)	–	–
Primary core	1881 (1.32×)	1109 (1.15×)	–	–
Secondary core	1897 (1.33×)	1059 (1.09×)	–	–
Conventional system	10964 (1.00×)	4181 (1.00×)	5.324	(1.00×)
Composable system	12522 (1.14×)	4517 (1.08×)	7.096	(1.33×)

[1] https://github.com/cliffordwolf/picorv32

Software

- Software Adaptation:

  An example of composed version of multi-precision addition

```
//Composed multi-precision addition
//input:  int *a_addr, int *b_addr,
//        int n_bytes, int n_cores
//output: int *r_addr
mp_add_com:
csrwi mcompose_mode, mcompose_wide
csrw  mcompose_reg,  n_cores
slli bytes_per_word, n_cores, 2

li   carry, 0
add  addr_end, n_bytes, a_addr
mp_add_comp_loop:
beq  a_addr,  addr_end, mp_add_end
lw   a_value, 0(a_addr)
lw   b_value, 0(b_addr)
add  r_value, a_value,  carry
sltu carry,   r_value,  a_value
add  r_value, r_value,  b_value
sltu t_carry, r_value,  b_value
or   carry,   carry,    t_carry
sw   r_value, 0(r_addr)
add  a_addr,  a_addr,   bytes_per_word
add  b_addr,  b_addr,   bytes_per_word
add  r_addr,  r_addr,   bytes_per_word
j    mp_add_comp_loop
mp_add_end:

csrw mcompose_reg, zero
ret
```

- Cryptographic software benchmarks:
  - Multi-precision algorithms: addition, multiplication, and modular exponentiation (modExp)
  - ChaCha20 stream cipher
  - AES-128 encryption

Performance Speed-up Results

- Speed up multi-precision algorithms using the wide data-path mode

1024-bit Operations	Metric	Single Core	Composed Systems	
			2 Cores	4 Cores
Addition	Instructions	431 (1.00×)	228 (1.89×)	124 (3.48×)
	Cycles	2023 (1.00×)	1225 (1.65×)	843 (2.40×)
Multiplication	Instructions	15822 (1.00×)	4083 (3.88×)	1091 (14.50×)
	Cycles	179395 (1.00×)	72490 (2.47×)	32086 (5.59×)
ModExp	Instructions	57395054 (1.00×)	15019653 (3.82×)	4144180 (13.85×)
	Cycles	594838395 (1.00×)	238293765 (2.50×)	106391562 (5.59×)

- Speed up ChaCha20 encryption in using the SIMD compute mode

Message size	Metric	OpenSSL	Single Core	Composed Systems		128 bit Vector [15]	
				2 Cores	4 Cores		
64 bytes	Instructions	2825 (1.00×)	1765 (1.60×)	1199 (2.36×)	659 (4.29×)	607	(4.65×)
	Cycles	25073 (1.00×)	17603 (1.42×)	11905 (2.11×)	7609 (3.30×)		
256 bytes	Instructions	11015 (1.00×)	6919 (1.59×)	4637 (2.38×)	2537 (4.34×)	2332	(4.72×)
	Cycles	98969 (1.00×)	69524 (1.42×)	46435 (2.13×)	29659 (3.34×)		
1024 bytes	Instructions	43775 (1.00×)	27535 (1.59×)	18389 (2.38×)	10049 (4.36×)	9232	(4.74×)
	Cycles	394553 (1.00×)	277208 (1.42×)	184555 (2.14×)	117859 (3.35×)		

Fault Detection Results

- Consider fault injection attacks on AES block cipher
  - Use the simulation-based to inject faults
  - 2 types of fault injections: control flow and data flow
  - Perform 100 times per experiment
  - AES encryption results are checked against the correct value,

    If failed, attacker takes advantage of the faults

- AES encryption against control flow and data fault injections

	Control flow fault case				Data fault case			
Implementations	Passed	Failed	Broken	Detected	Passed	Failed	Broken	Detected
Unprotected AES	30	62	8	–	42	29	29	–
Protected AES	12	0	2	87	46	0	0	54

Concluding Remarks

- A proof-of-concept multi-core processor implemented on a FPGA platform
  - Present a Composable Lightweight Processor to support cryptographic workloads
  - General-purpose benefits of a multi-core processor
  - Flexible composed modes to address pertinent efficiency or security challenges
- Furture Works
  - Explore and address system-level challenges
  - Address obvious drawbacks, e.g., the increased critical delay in Wide Data-path
  - Consider other base-cores, e.g., a pipelined processor instead of PicoRV32
- Open-Source: https://github.com/scarv/hydra

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