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# From Swift to Mighty: A Cost-Benefit Analysis of Ibex and CV32E40P Regarding Application Performance, Power and Area

**CARRV Workshop, June 17th, 2021**

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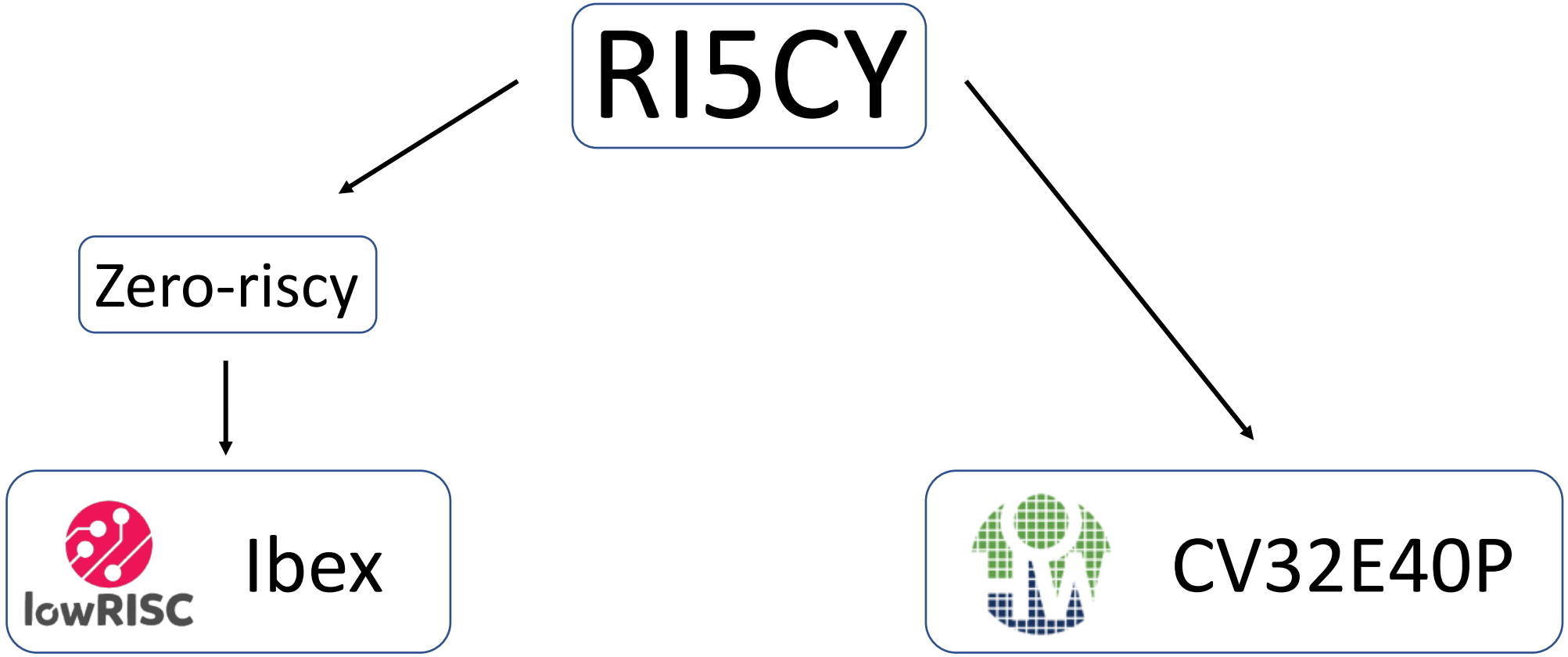
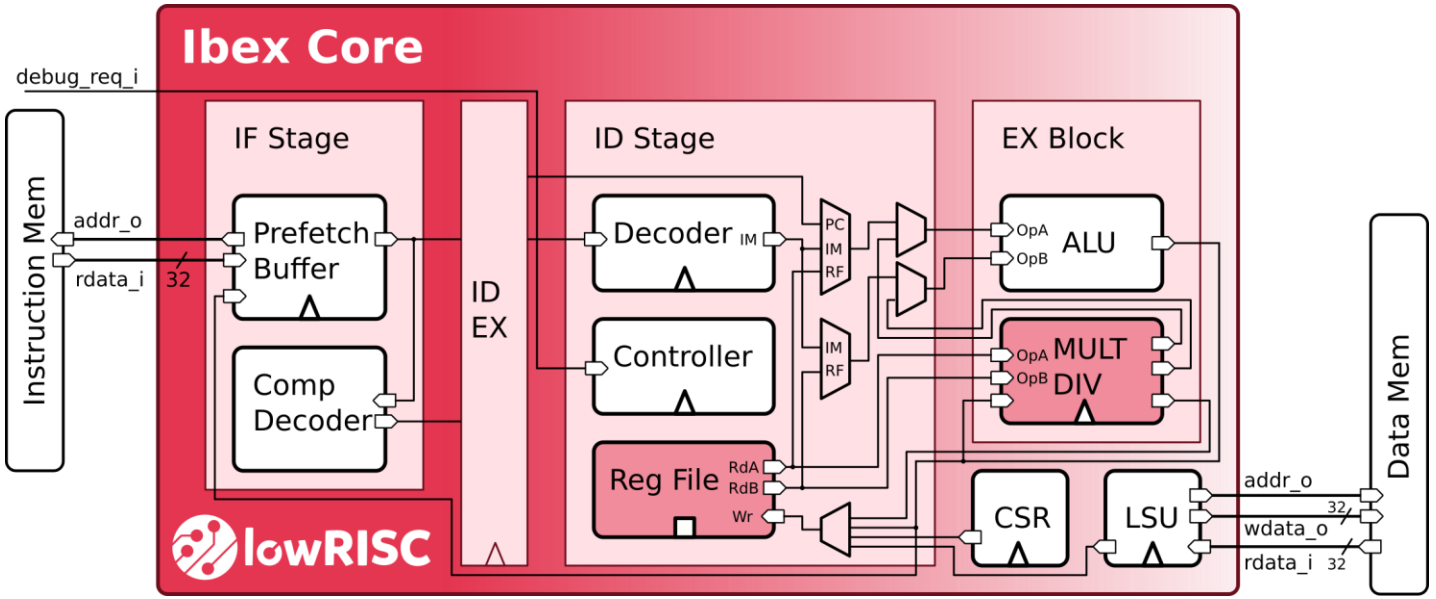
# A Tale of Two Cores



# Contributions of this Work

- **Application performance** analysis
- Silicon **Area** comparison
- **Power** and **energy efficiency** estimation
- **Cost-benefit analysis** of different **RTL configurations**

# Ibex: The Little Brother



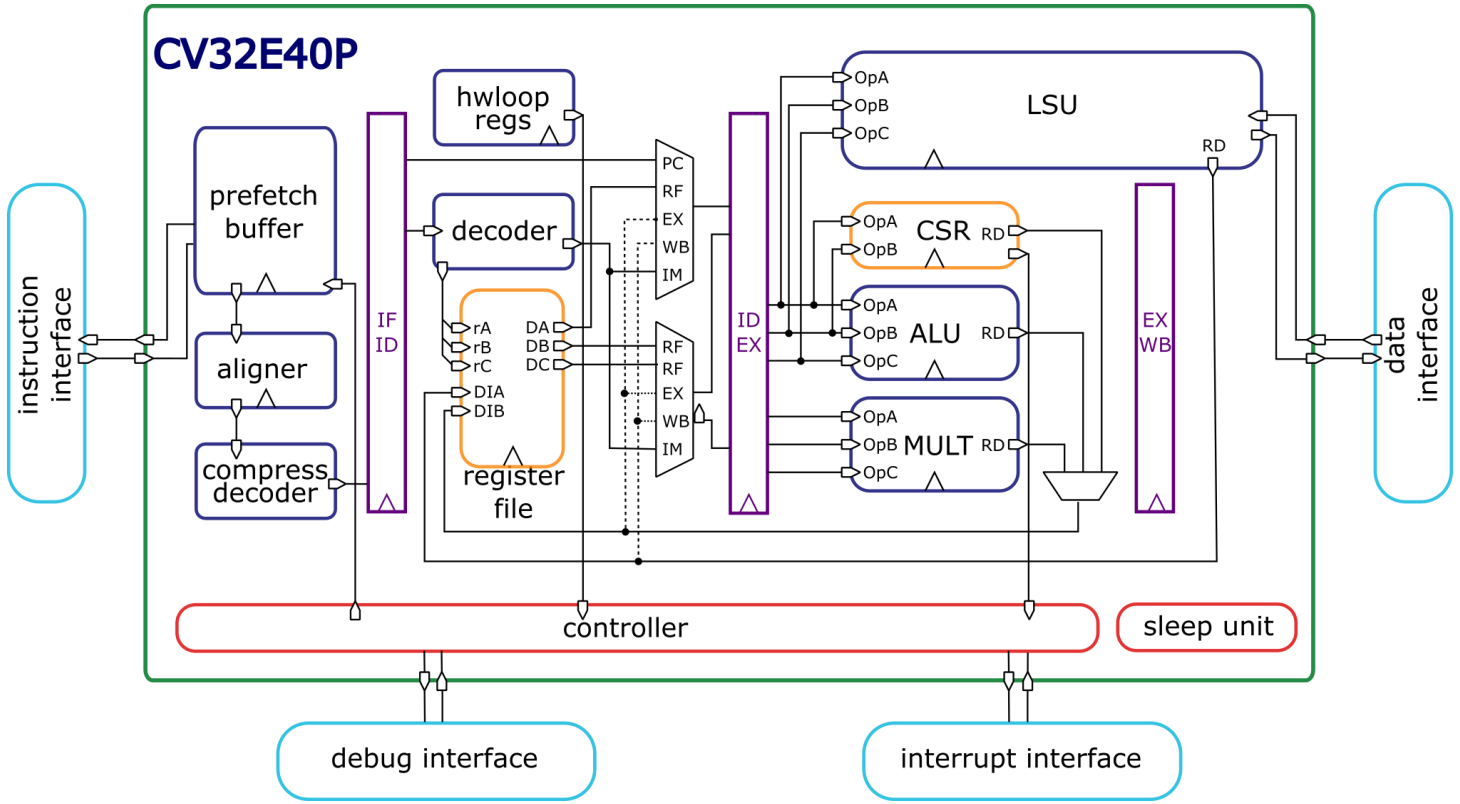

**ISA:**

- RV32I[M]C

**Configuration Options**

- Writeback Stage (WB-Stage)
- Branch Target ALU (BT-ALU)
- Static Branch Predictor (SBP)
- Single-Cycle Multiplier (SC-Mult)

# CV32E40P: The Big Brother




**ISA:**

- RV32IM[F]C_Xpulp

**Features**

- Zero-overhead loops
- Post-modifying memory operations
- Dot-product instructions
- Single-instruction-multiple-data (SIMD) instructions

# Experimental Setup: Area, Frequency and Power

**Synthesis:**

- TSMC 65nm with typical case conditions (1.2V, 25°C) using Synopsys DC
- Latch-based register file implementation for both cores
- Timing constraint: delay of 40% of clock period on all inputs and outputs

**Power estimations:**

- Simulation of post-synthesis netlist
- Switching activity analysis while executing CoreMark using Synopsys PrimeTime

# Experimental Setup: Benchmark Programs

**CoreMark:**
Stand-alone industry standard benchmark for embedded processors

**Workload:** List processing, matrix multiplications, state machine, cyclilc redundancy tests

**Score:**
- **Summary**: Number of Iterations per Second [CoreMark]

**Embench:**
Collection of 19 programs taken from real-world applications

**Workload:** Varying emphasis of the different programs

**Score:**
- **Per program**: Execution time relative to ARM Cortex-M4*
- **Summary**: geometric mean across all 19 programs.

# Experimental Setup: Compilers

**Ibex Maximum Performance:**

**ISA**: RV32IMC

**Compiler:** Upstream GCC 10.2.0

**CV32E40P vs. Ibex:**

**ISA:** RV32IM (Ibex), RV32IM_Xpulp (CV32E40P)

**Compiler:** Modified PULP toolchain (GCC 7.1.1)

| Target Binary | Toolchain Options | Relative Code Size (Embench) |
|---|---|---|
| Size optimized | -Os + garbage collection | 1x |
| Balanced (Embench baseline) | -O2 + garbage collection | 1,15x |
| Balanced - High performance | -O3 + garbage collection | 1,60x |
| High performance | -O3 + loop unrolling + garbage collection | 2,60x |
| Maximum Performance | -O3 + alignment + loop unrolling | 5,38x |

# Core Area and Frequency

| Core Config | Area [kGE] @ 100 Mhz | | @ max. Freq. | | Max. Freq. [MHz] |
|---|---|---|---|---|---|
| | Area | Delta | Area | Delta | |
| Ibex Default | 23,72 | - | 31,47 | - | 500 |
| + SBP | 25,41 | +1,69 (+7%) | 31,60 | +0,13 (+0%) | 391 (-22%) |
| +SC-Mult | 27,40 | +3,68 (+15%) | 41,87 | +10,40 (+33%) | 493 (-1%) |
| + BT-ALU | 24,16 | +0,44 (+2%) | 29,82 | -1,65 (-5%) | 420 (-16%) |
| +WB-Stage | 24,65 | +0,92 (+4%) | 32,99 | +1,52 (+5%) | 496 (-1%) |
| Ibex + All | 30,36 | +6,64 (+28%) | 37,04 | +5,57 (+18%) | 394 (-21%) |
| CV32E40P | 53,64 | +29,92 (+126%) | 71,99 | +40,52 (+129%) | 453 (-9%) |

# Ibex Maximum Performance: IPC

| Compiler Config | Embench / CoreMark per MHz | | | | | |
|---|---|---|---|---|---|---|
| | Default | SBP | SC-Mult | BT-ALU | WB-Stage | All |
| Size optimized | 0,71 / 1,58 | 0,73 / 1,58<br>+2,8% / -0,2% | 0,74 / 1,63<br>+4.2% / +3.1% | 0,75 / 1,71<br>+5,6% / +7,6% | 0,81 / 1,75<br>+14,1% / +10,3% | 0,91 / 1,96<br>+28,3% / +23,7% |
| Balanced | 0,76 / 2,07 | 0,78 / 2,20<br>+2,6 % / +6,4 % | 0,79 / 2,15<br>+3,9% / +4,0% | 0,79 / 2,23<br>+3,9% /+7,6% | 0,88 / 2,31<br>+15,8% / +11,6% | 1,00 / 2,79<br>+31,6% / +34,9% |
| Balanced – H. perf. | 0,81 / 2,19 | 0,84 / 2,30<br>+3,7% / +5,1% | 0,85 / 2,29<br>+4,9% / +4,3% | 0,85 / 2,35<br>+4,9% / +7,2% | 0,94 / 2,46<br>+16,0% / +12,0% | 1,07 / 2,94<br>+32,1% / +34,1% |
| High performance | 0,86 / 2,35 | 0,87 / 2,43<br>1,2% / +3,6% | 0,90 / 2,46<br>+4,7% / +4,6% | 0,88 / 2,49<br>+2,3% / +6,2% | 1,00 / 2,65<br>+16,3% / +13,0% | 1,12 / 3,12<br>+30,2% / +33,0% |
| Max. performance | 0,87 / 2,36 | 0,88 / 2,44<br>+1,1% / +3,3% | 0,92 / 2,47<br>+5,7% / +4,6% | 0,90 / 2,51<br>+3,4% / +6,3% | 1,02 / 2,67<br>+17,2% / 13,1% | 1,14 / 3,17<br>+31,0% / +34,1% |



**ISA:** RV32IMC, **Compiler:** Upstream RISC-V GCC (10.2.0)

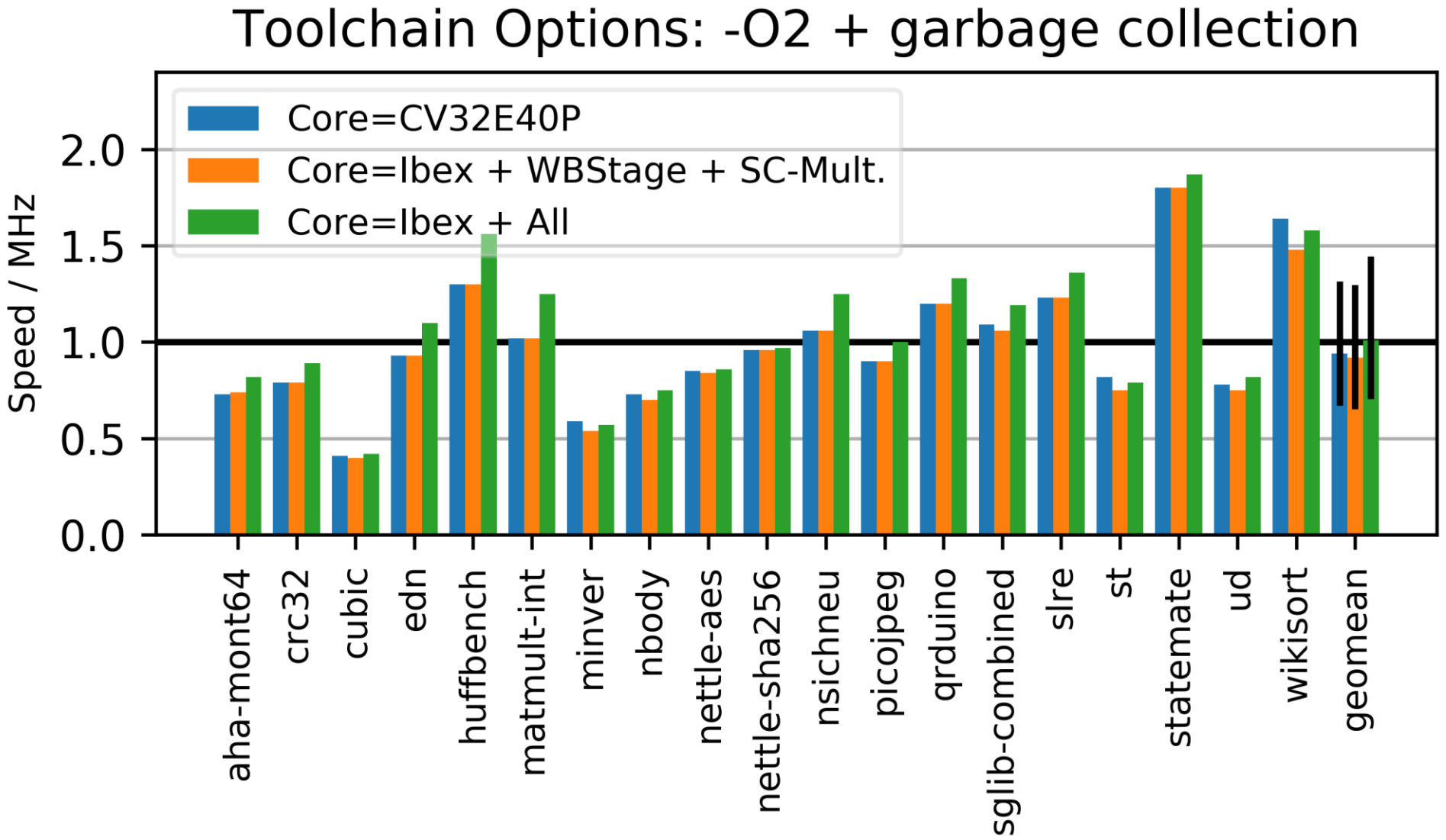
# Ibex Maximum Performance: @max. Frequency

| Compiler Config | Embench / CoreMark @maximum Frequency | | | | | |
|---|---|---|---|---|---|---|
| | Default @500 MHz | SBP @391 MHz | SC-Mult @493 MHz | BT-ALU @420 MHz | WB-Stage @496 MHz | All @394 MHz |
| Size optimized | 354 / 791 | 285 / 618<br>-19,5% / -21,9% | 365 / 805<br>+2,9% / +1,8% | 315 / 718<br>-11,1% / -9,3% | 401 / 867<br>+13,3% / +9,6% | 358 / 772<br>+1,1% / -2,4% |
| Balanced | 379 / 1034 | 304 / 861<br>-19,7% / -16,7% | 389 / 1063<br>+2,7% / +2,8% | 331 / 937<br>-12,6% / -9,5% | 436 / 1147<br>+15,0% / +10,9% | 393 / 1101<br>+3,8% / +6,4% |
| Balanced – H. perf. | 404 / 1096 | 328 / 901<br>-18,8% / -17,8% | 419 / 1128<br>+3,6% / +3,0% | 357 / 988<br>-11,7% / -9,8% | 466 / 1219<br>+15,3% / +11,3% | 421 / 1160<br>+4,2% / +5,9% |
| High performance | 429 / 1173 | 340 / 951<br>-20,8% / -18,9% | 443 / 1212<br>+3,4% / +3,3% | 369 / 1048<br>-13,9% / -10,7% | 496 / 1316<br>+15,5% / +12,2% | 441 / 1230<br>+2,7% / +4,9% |
| Max. performance | 434 / 1179 | 344 / 953<br>-20,8% / -19,1% | 453 / 1218<br>+4,4% / +3,3% | 378 / 1053<br>-13,0% /-10,6% | 506 / 1324<br>+16,5% / +12,3% | 449 / 1247<br>+3,3% / +5,8% |



**ISA:** RV32IMC, **Compiler:** Upstream RISC-V GCC (10.2.0)

# Ibex vs. CV32E40P: IPC, No Xpulp Extension








**ISA:** RV32IMC, **Compiler:** Upstream RISC-V GCC (10.2.0)

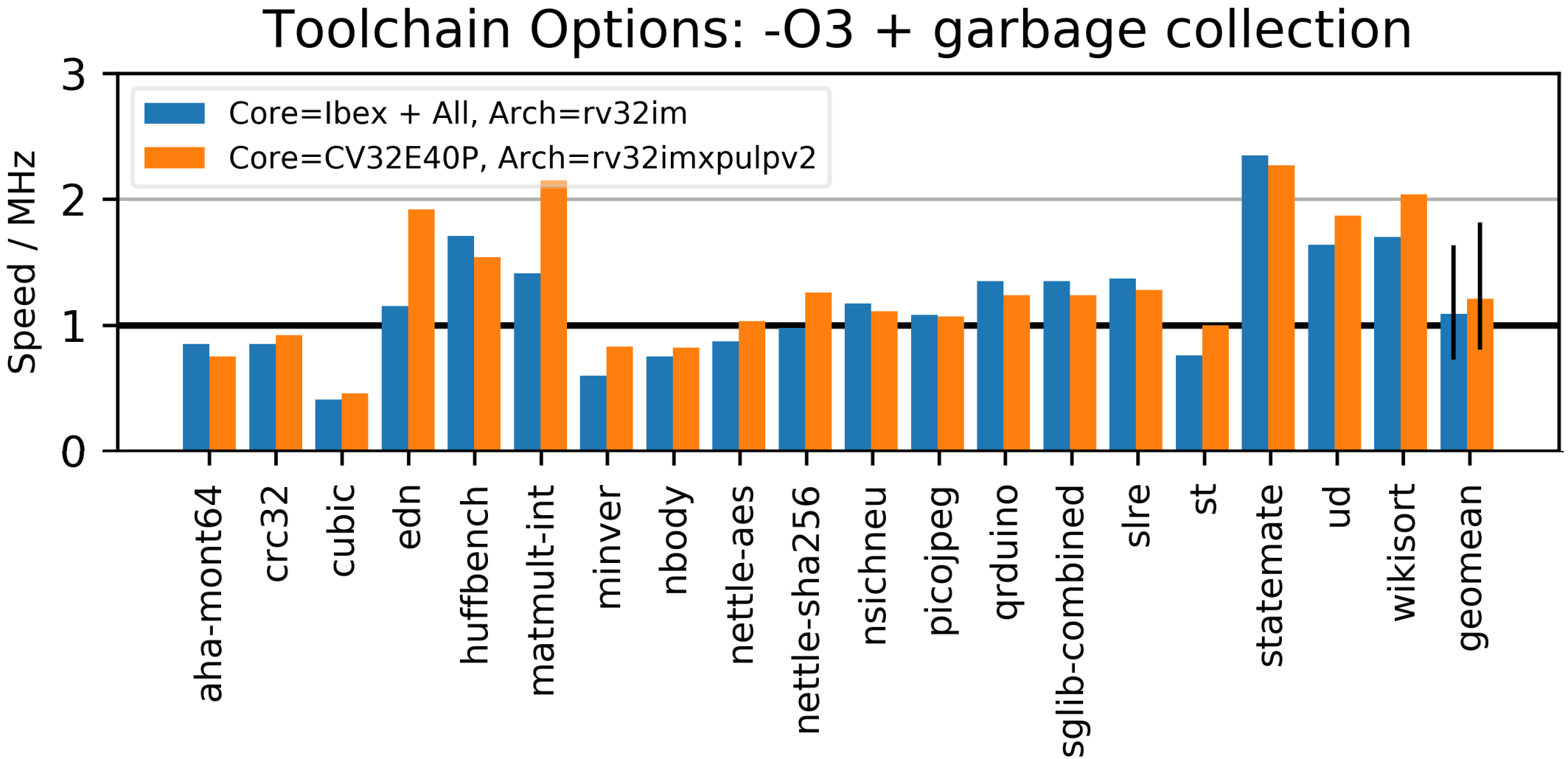
# Ibex vs. CV32E40P: With Xpulp Extensions

| Compiler Config | Embench / CoreMark Scores | | | |
|---|---|---|---|---|
| | Ibex + All (IPC Perf.) | CV32E40P (IPC Perf.) | Ibex + All @394 MHz | CV32E40P @453 MHz |
| Size optimized | 0,94 / 1,96 | 1,05 / 1,98<br>+11,7% / +1,1% | 370 / 772 | 475 / 897<br>+28,4% / +16,2% |
| Balanced | 1,00 / 2,79 | 1,11 / 2,74<br>+11,0% / +27,6% | 393 / 1101 | 502 / 1239<br>+27,6% / +12,6% |
| Balanced – H. perf. | 1,09 / 2,94 | 1,21 / 3,06<br>+11,0% / +4,0% | 429 / 1160 | 547 / 1387<br>+27.6% / +19,6% |
| High performance | 1,15 / 3,12 | 1,23 / 3,11<br>+7,0% / -0,6% | 452 / 1230 | 556 / 1406<br>+22,9% / 14,3% |



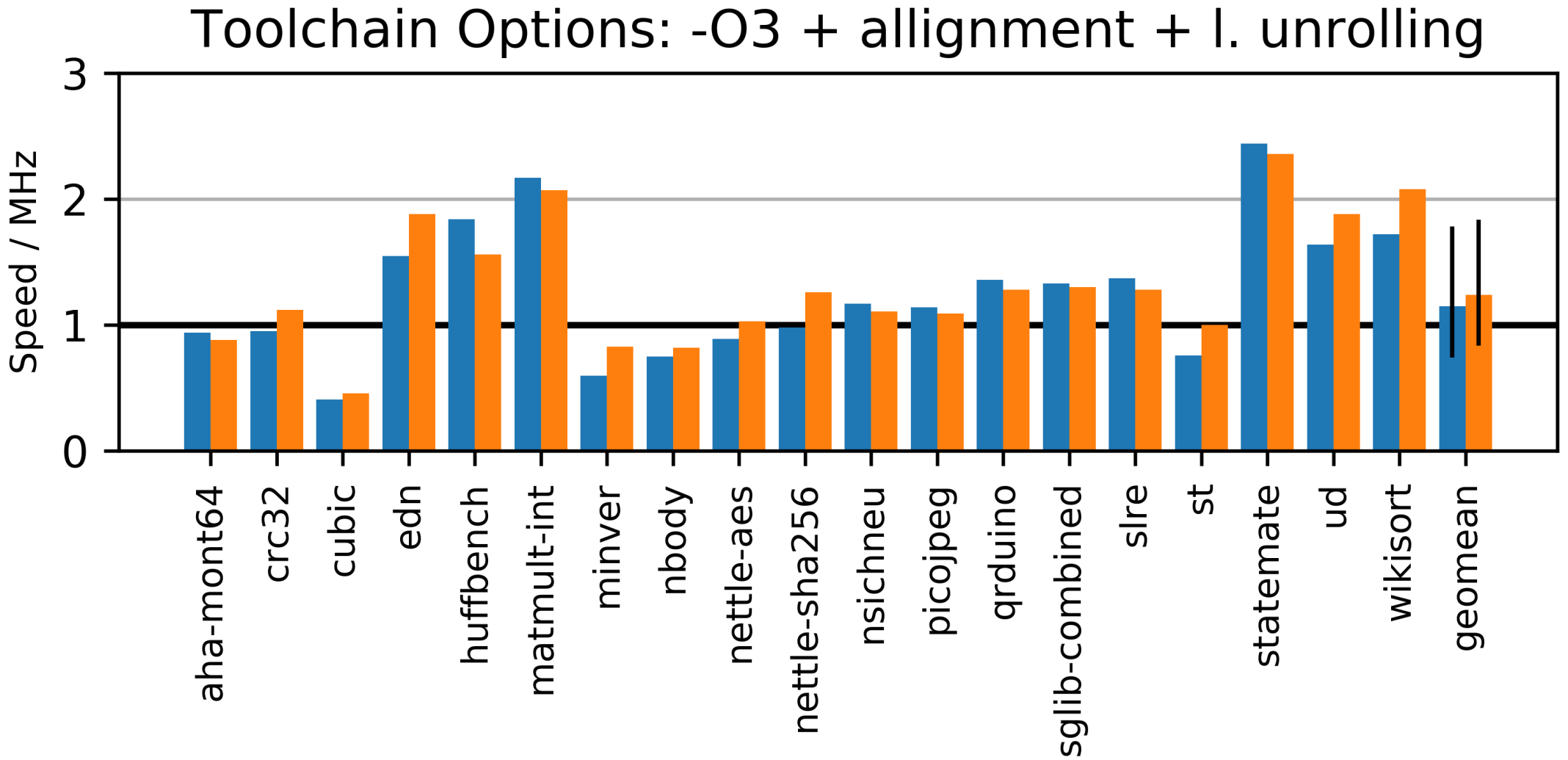
**ISA:** RV32IM (Ibex), RV32IM_Xpulp (CV32E40P), **Compiler:** Modified PULP GCC (7.1.1)

# Ibex vs. CV32E40P: Detailed View




**ISA:** RV32IM (Ibex), RV32IM_Xpulp (CV32E40P), **Compiler:** Modified PULP GCC (7.1.1)

# Ibex vs. CV32E40P: Detailed View




**ISA:** RV32IM (Ibex), RV32IM_Xpulp (CV32E40P), **Compiler:** Modified PULP GCC (7.1.1)

# Power and Energy Efficiency (CoreMark)

| | Power (Dyn.[mW]/ Lkg [$\mu$W]) | | Energy per Iteration (Dyn[$\mu$ J] / Lkg [nj]) | |
|---|---|---|---|---|
| **Core Config** | **@100 MHz** | **@max. Freq.** | **@ 100 MHz** | **@max. Freq.** |
| Ibex (500 MHz) | 0,80 / 0,18 | 1,09 / 6,53 | 3,40 / 0,75 | 0,92 / 5,54 |
| + SBP | 0,88 / 0,20<br>+9,1% / +15,2% | 1,16 / 6,42<br>+6,8% / -1,7% | 3,59 / 0,84<br>+5,6% / +11,5% | 1,22 / 6,74<br>+32,1% / +21,6% |
| + SC-Mult | 0,98 / 0,19<br>+22,7% / +7,9% | 1,44 / 13,80<br>+32,3% / +111,3% | 3,99 / 0,78<br>+17,3% / +3,1% | 1,18 / 11,34<br>+28,0% / +104,6% |
| + BT-ALU | 0,84 / 0,18<br>+5,4% / +2,8% | 1,08 / 6,03<br>-0,7% / -7,7% | 3,37 / 0,73<br>-0,8% / -3,2% | 1,03 / 5,72<br>+11,1% / +3,3% |
| + WB-Stage | 0,96 / 0,19<br>+20,0% / +7,9% | 1,32 / 7,59<br>+21,7% / +16,2% | 3,61 / 0,72<br>+6,1% / -4,6% | 1,00 / 5,74<br>+8,4% / +3,5% |
| Ibex + All | 1,33 / 0,37<br>+65,3% / +27,0% | 1,78 / 9,59<br>+63,3% / +46,9% | 4,22 / 0,72<br>+24,2% / -4,6% | 1,44 / 7,75<br>+55,5% / +39,8% |
| CV32E40P | 1,36 / 0,37<br>+69,8% / +27,0% | 1,57 / 18,80<br>+44,2% / +187,9% | 4,39 / 1,20<br>+29,0% / +58,8% | 1,12 / 13,37<br>+20,9% / +141,3% |

**Ibex: ISA:** RV32IMC, **Compiler:** Upstream RISC-V GCC (10.2.0)
**CV32E40P: ISA:** RV32IM_XPULP **Compiler:** Modified PULP GCC (7.1.1)

# Conclusion

- **Ibex** is well suited for a **versatile** range of workloads
  - Performance-enhancing features **trade IPC performance for silicon area**
  - CoreMark **IPC performance** increases **up to +34%** at **area cost of +18% to +28%** depending on timing target
  - **Limited net performance increase (+6%)** due to **impact on critical path** by branch target ALU and static branch predictor
- **Power-Performance-Area comparison** between Ibex and CV32E40P
  - Using **baseline (RV32IMC) ISA**, **net performance is comparable at a 40% lower area**
  - Including **Xpulp extensions**, Ibex can achieve **similar performance** levels as CV32E40P through compile-time optimizations at the cost of **heavily inflated code size.**
  - **CV32E40P** at a **clear advantage** for highly regular, **compute intensive applications**
- Default **Ibex** remains the **most energy-efficient** option
  - Identified potential for energy efficiency improvements for Ibex.

# The End

**Thanks for your Attention!**