



# Leveraging RISC-V to build an open-source (hardware) OS framework for reconfigurable IoT devices

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# TABLE OF CONTENTS

## Motivation

Internet of Things, Reconfigurable Platforms, RISC-V

## ChamelloT

Architecture, Proof-of-Concept Implementation

## Preliminary Results

Hardware Resources, Determinism and Performance

## Roadmap & Conclusion

Next steps, Final remarks

# Motivation

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03 Jan 2019

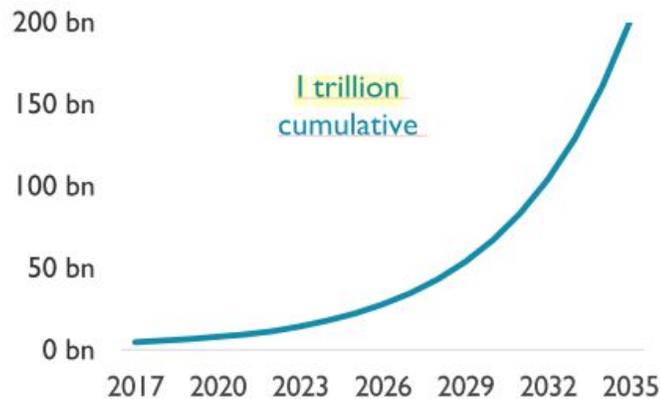
IDC Forecasts Worldwide Spending on the Internet of Things to Reach \$745 Billion in 2019, Led by the Manufacturing, Consumer, Transportation, and Utilities Sectors

EGHAM, U.K., August 29, 2019

**Gartner Says 5.8 Billion Enterprise and Automotive IoT Endpoints Will Be in Use in 2020**

# THE INTERNET OF THINGS

Annual Production of IoT devices



**Popular Internet of Things Forecast of 50 Billion Devices by 2020 Is Outdated**

Warning: All projections for the Internet of Things are subject to change

# RECONFIGURABLE PLATFORMS

As FPGAs get **bigger**, **faster**, and **cheaper**, their presence in the embedded systems market expands.

In the IoT industry, these platforms are also gaining traction due to the **performance**, **flexibility**, and **scalability** they provide.

CUTE Mote, A Customizable and Trustable End-Device for the Internet of Things

Arnold: An eFPGA-Augmented RISC-V SoC for Flexible and Low-Power IoT End Nodes

The migration of OS kernel services **failed** in being adopted due to the overwhelming presence of proprietary processor IPs.

Based IoT End Nodes

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\*Department of Electrical, Electronic and Information Engineering (DEI), University of Bologna, Italy  
†IIS Integrated Systems Laboratory, ETH Zurich, Switzerland

The quick and safe way to build secure IoT applications with any RISC-V processor

Cesare Garlati – Hex Five Security  
Sandro Pinto – Hex Five Security

# CHAMELIOT

**ChamelloT** is an **agnostic hardware OS framework** for reconfigurable IoT platforms.

By leveraging the RISC-V architecture, ChamelloT goals include providing:

- Real-time and Determinism
- Performance
- Agnosticism
- Flexibility and Portability
- Power Consumption



Motivation

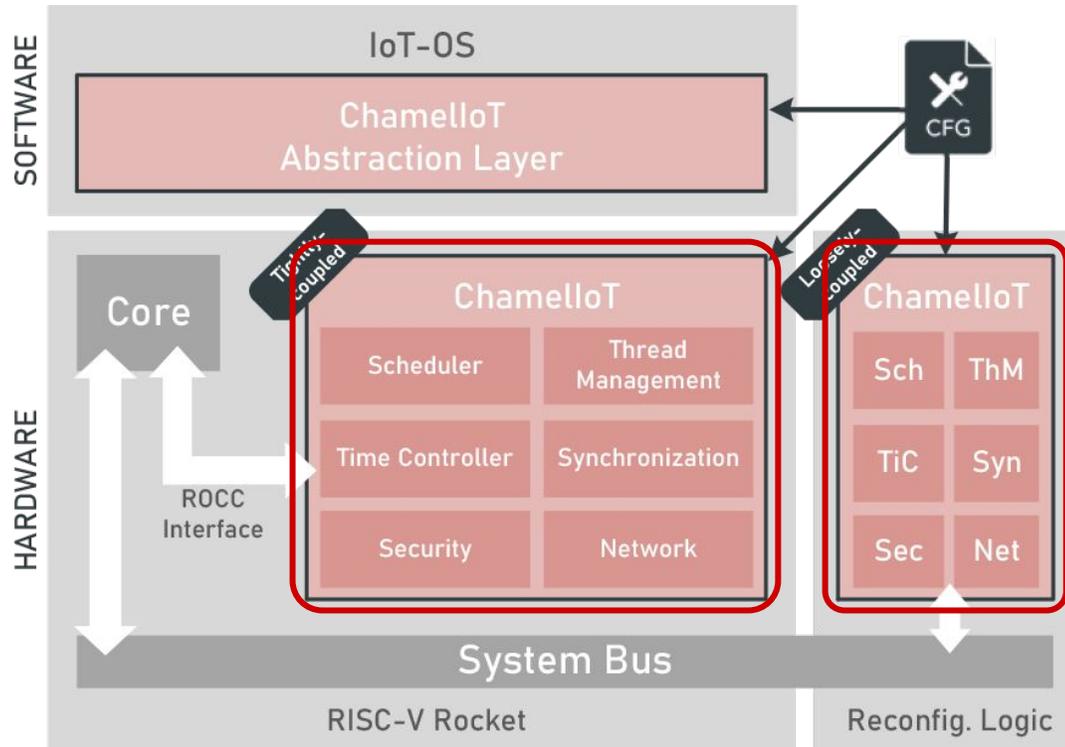
# ChamelloT

Architecture, Proof-of-Concept Implementation

Preliminary Results

Roadmap & Conclusion

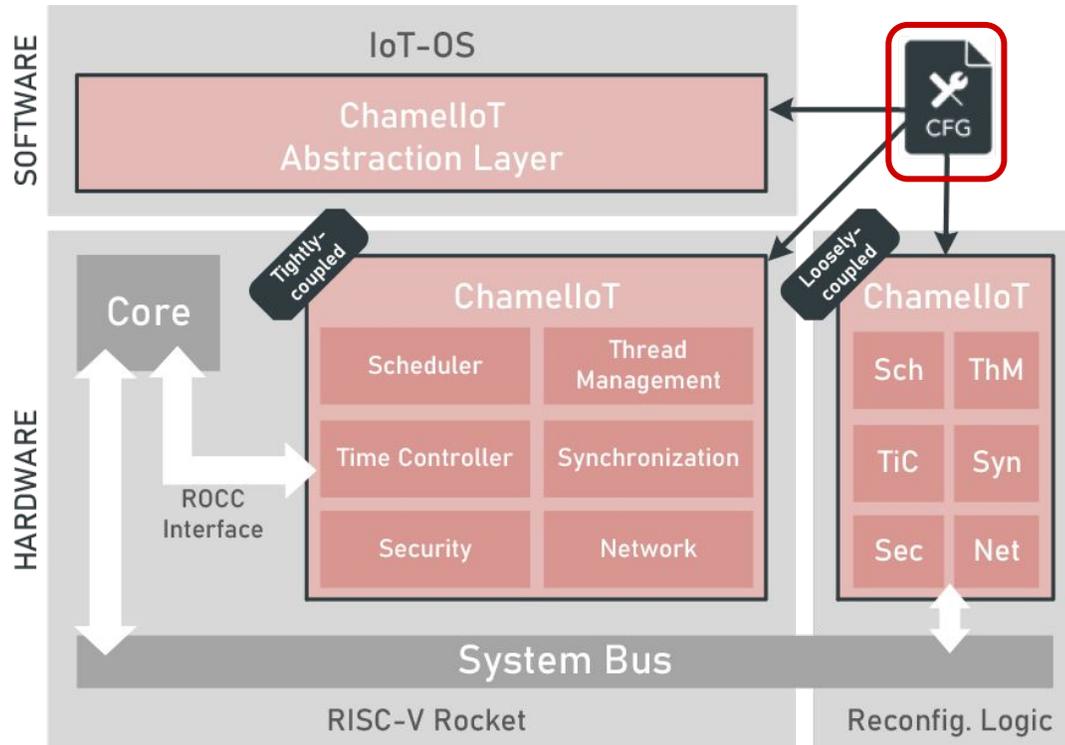
# CHAMELIOT ARCHITECTURE



ChamelloT's hardware component main focus is to accelerate OS kernel services.

ChamelloT aims at exploring the trade-offs between tightly- and loosely-coupled architectures.

# CHAMELIOT ARCHITECTURE

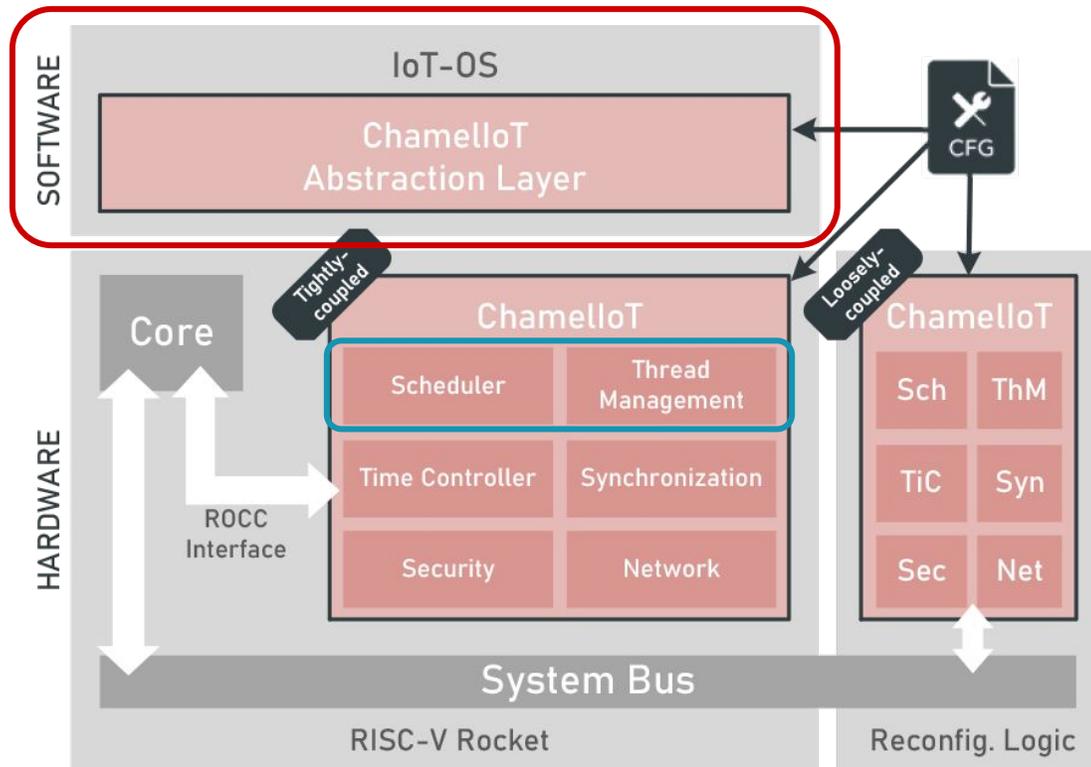


The *External Configuration Tool* can be used to configure and fine-tune the full system.

- Kernel components;
- Fine-grain features of system components;
- Configurations, e.g. tightly- vs loosely-coupled.

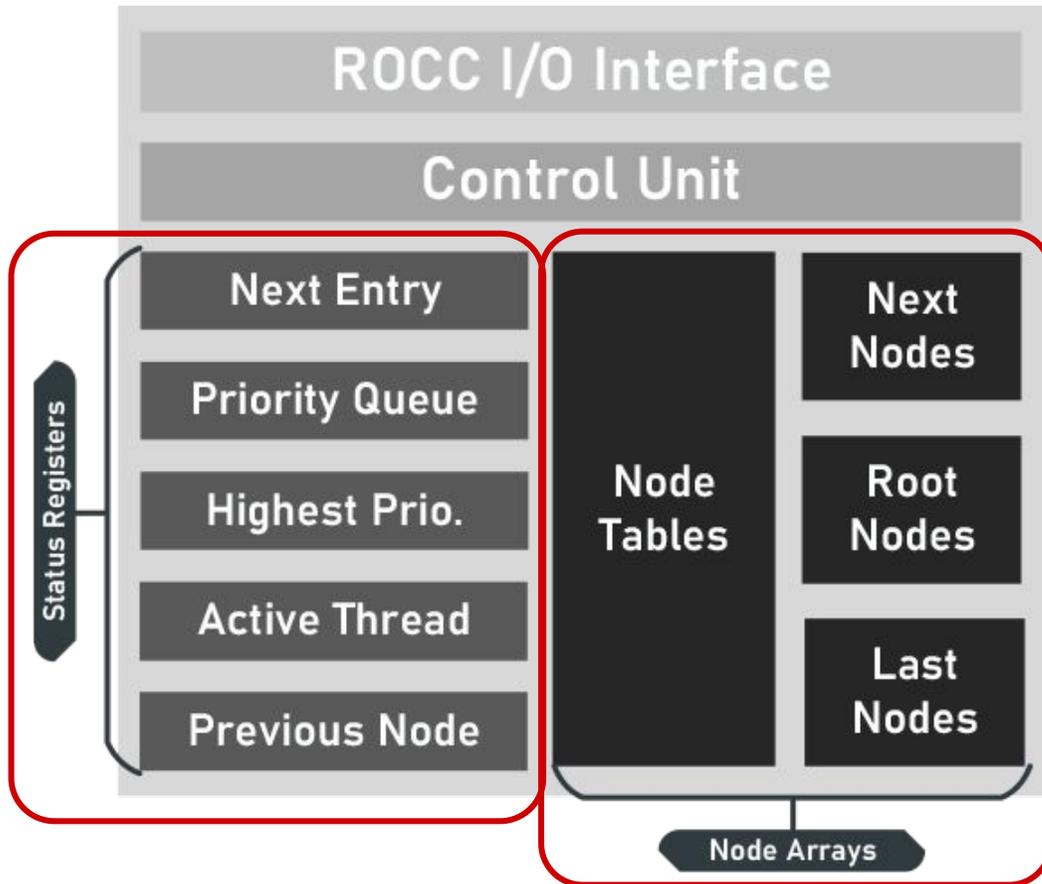
# CHAMELIOT ARCHITECTURE

*ChamelloT Abstraction Layer* aims at providing agnosticism for applications targeting different OSes.



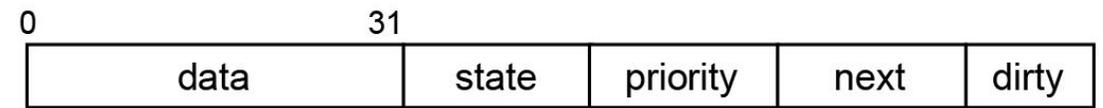
Key aspects	RIOT	Zephyr	FreeRTOS
Ready Queue	Multi-queue	Multi-queue	Multi-queue
States	14	8	4
<i>Scheduling Points</i>	Tickless	Tickless	Tick-based
Priority	Descending	Descending	Ascending

# PROOF-OF-CONCEPT IMPLEMENTATION



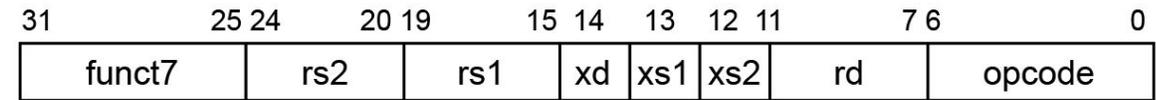
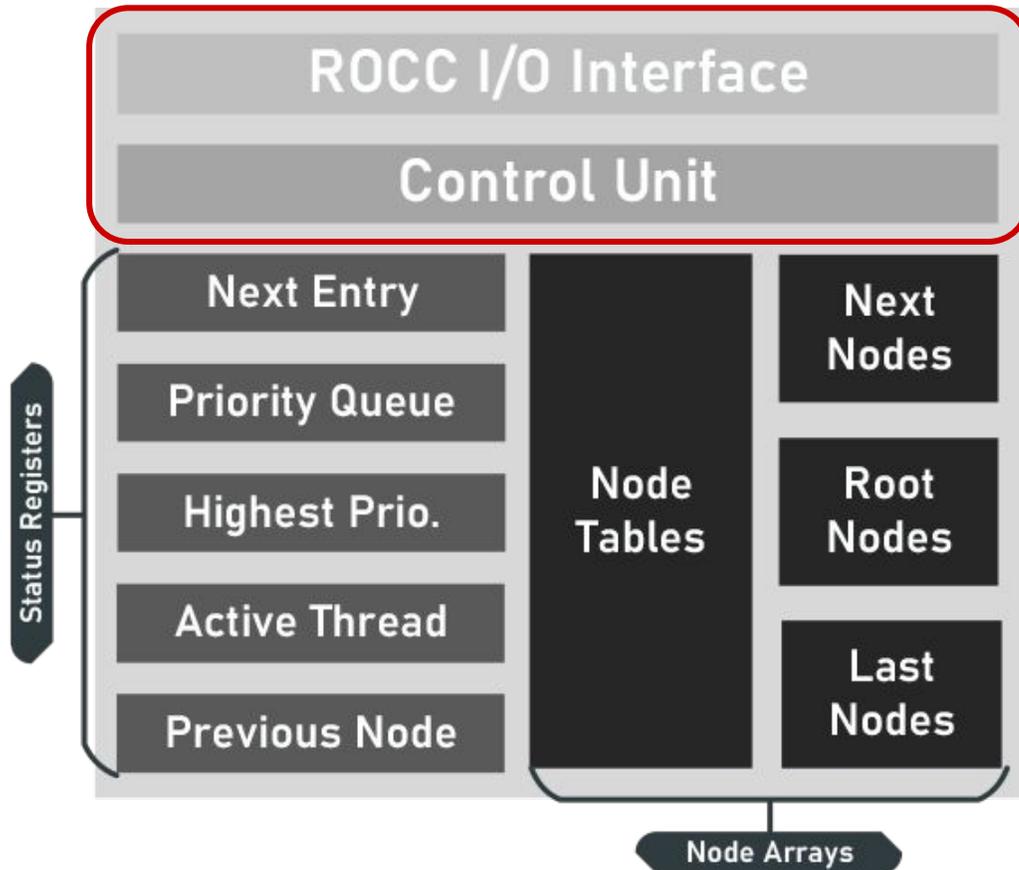
*Status Registers* are used to keep track of the state of the multiple linked lists.

*Node Arrays* are sets of nodes and registers that constitute the linked lists



Linked-List Node

# PROOF-OF-CONCEPT IMPLEMENTATION



RoCC Instruction Format

Function	<i>funct7</i>	<i>rs1</i>	<i>rs2</i>	<i>rd</i>	Description
Add	0	priority	TCB	TID	Adds a thread to the table
Remove	1	TID	none	none	Removes a thread from the table
Active PID	2	none	none	TID	Returns the TID of the running thread
Get TCB	3	TID	none	TCB	Returns the thread TCB
Schedule	4	none	none	TID	Schedules and sets the state of the next thread; changes the state of the current active thread
Set State	5	TCB	state	none	Changes the thread state (might cause ChamellIoT to move the thread to/from the ready queue)
Get PID	6	TCB	none	TID	Returns the thread PID

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ChamelloT

**Preliminary Results**

Hardware Resources, Determinism and Performance

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# HARDWARE RESOURCES

ChamelloT PoC implementation was deployed and evaluated on a SiFive Freedom E300 in a Xilinx Arty-35T FPGA board.

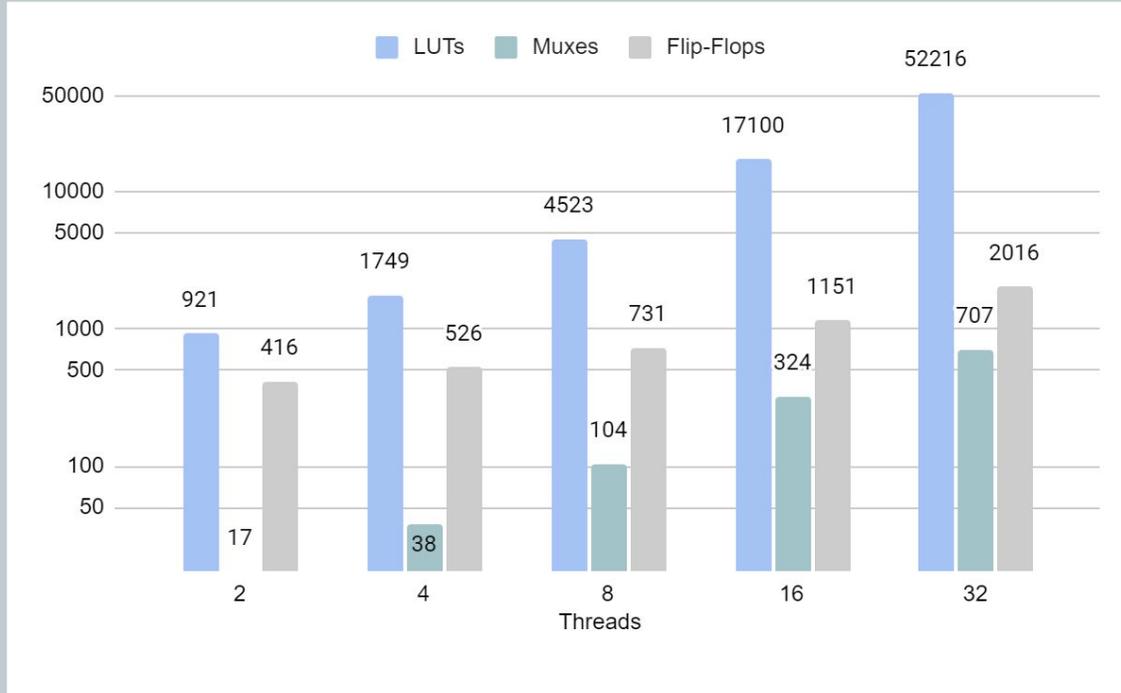
- The base configuration supported a total of 8 threads and 8 priority levels:

Resource	Rocket	Rocket + RoCC	Rocket + ChamelloT
LUTs	17246	17791 (+3.16%)	21769 (+26.23%)
MMCM	1	1 (+0%)	1 (+0%)
Muxes	381	403 (+5.77%)	485 (+27.3%)
RAM	197	229 (+16.24%)	240 (+21.83%)
SRL	89	89 (+0%)	89 (+0%)
FFs	10096	10362 (+2.63%)	10827 (+7.24%)
IOBUF	58	58 (+0%)	58 (+0%)

# HARDWARE RESOURCES

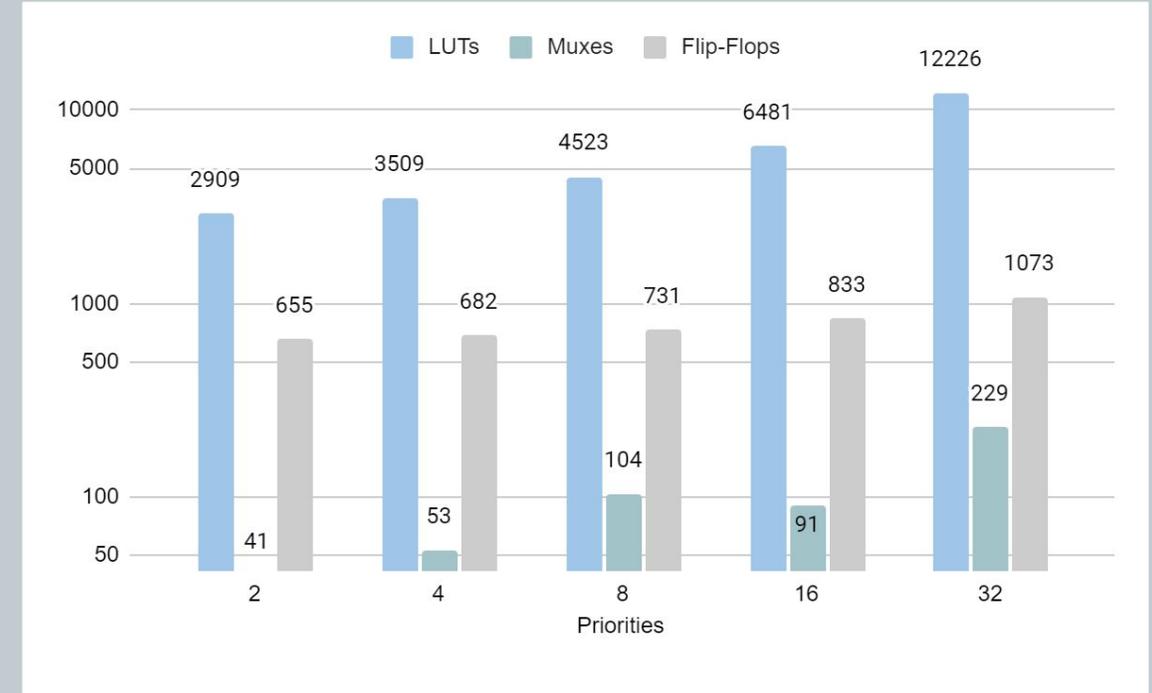
## Fixed number of priorities (8)

Varying the number of **threads**



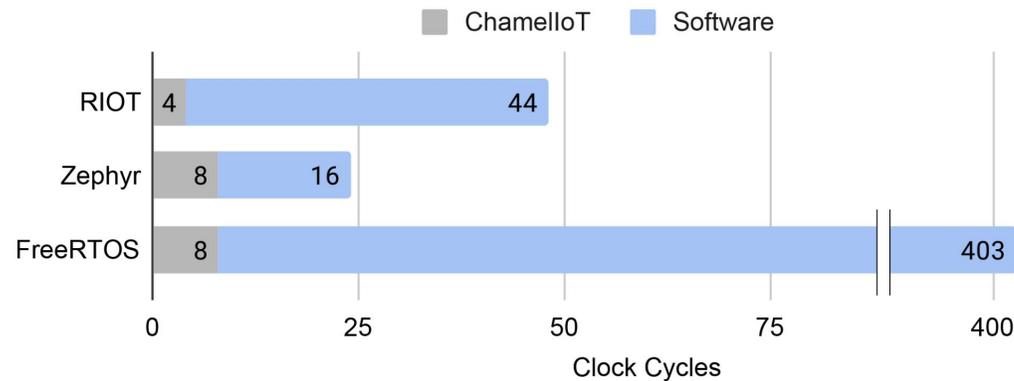
## Fixed number of threads (8)

Varying the number of **priorities**



# DETERMINISM & PERFORMANCE

We have measured the number of clock cycles required to perform the thread selection algorithm.



- RIOT and FreeRTOS vastly benefit from using ChamelloT scheduler.
- Despite the impact of ChamelloT on Zephyr being lesser, our past research proved that Zephyr will benefit from ChamelloT in other areas.

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# NEXT STEPS

## Hardware

Thread Management

Timing Control

Synchronization and IPC

Loosely-coupled Accelerator

## Software

Operating Systems Integration

Configuration Tool

# TAKE AWAYS

1

Accelerating OS kernel services with ChamelloT brings several benefits in terms of performance and determinism

2

ChamelloT can be configured to perfectly fit the system's needs

3

Research will focus on providing support to a broader number of kernel features and additional OSes

# THANK YOU!

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Q&A