OpenPiton + Ariane 🚀:
The First Open-Source SMP Linux-booting RISC-V System
Scaling From One to Many Cores

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Princeton University, ETH Zurich

openpiton.org
pulp-platform.org
Who are we?

• Jonathan Balkind
  • Lead architect of OpenPiton

• OpenPiton Team
  • Led by Prof. David Wentzlaff
  • Princeton Parallel Research Group
  • Open source HW since 2015
  • 13 PhD students
  • 1 Postdoc
  • N undergraduates

• Michael Schaffner
  • Responsible for OpenPiton+ Ariane integration

• PULP Team
  • Led by Prof. Luca Benini
  • ETHZ / Università di Bologna
  • Open source HW since 2013
  • Leaders in RISC-V development
  • Ariane dev: Florian Zaruba, Michael Schaffner and others
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Project Overview

• Collaboration between Princeton University and ETH Zurich

• Goal is to develop a permissively licensed, Linux capable manycore research platform based on RISC-V
  • Based on mature, extensible designs
  • Booted SMP Linux in <6 months
  • The world's first open-source, SMP Linux-booting, RISC-V manycore

• Ariane
  • RV64GC Core (with extensions)
  • Linux capable

• OpenPiton
  • Manycore research platform
  • Distributed cache coherence and NoC
Ariane RV64GC Core

- Application class processor
  - Written in SystemVerilog
- Linux Capable
  - Tightly integrated D$ and I$
  - M, S and U privilege modes
  - TLB, SV39
  - Hardware PTW
- Optimized for performance
  - Frequency: 1.5 GHz (22 FDX)
  - Area: ~ 175 kGE
  - Critical path: ~ 25 logic levels

- Scoreboarding
- 6-stage pipeline
  - In-order (single) issue
  - Out-of-order write-back
  - In-order commit
- Designed for extensibility
- Branch-prediction
  - Return Address Stack (RAS)
  - Branch Target Buffer (BTB)
  - Branch History Table (BHT)
Ariane
Silicon Proven Designs: Ariane

- **Ariane** taped-out in **GlobalFoundries 22nm FDX** twice
- 16kB instruction and 32kB data caches
- Poseidon:
  - Area: 0.23 mm² - 175 kGE
  - 0.2 - 1.7 GHz (0.5 V - 1.15 V)
- Kosmodrom:
  - RV64GCXsmallFloat, Transprecision / Vector FPU
  - **Ariane HP**
    - 8T library, 0.8V, 1.3 GHz
    - 55 mW @ 1 GHz
  - **Ariane LP**
    - 7.5T ULP library, 0.5V, 250 MHz
    - 5 mW @ 200 MHz
OpenPiton

- Open source manycore
- Written in Verilog RTL
- P-Mesh coherence scales to ½ billion cores
- Configurable core, uncore
- Simulation in VCS, ModelSim, Incisive, Verilator, Icarus
- Includes synthesis and back-end flow
- ASIC & FPGA verified
- ASIC power and energy fully characterized [HPCA 2018]
- Runs full stack multi-user Debian Linux
- Used for Architecture, Programming Language, Compilers, Operating Systems, Security, EDA research
OpenPiton Tile

- L2 Cache Slice + Directory Cache
- P-Mesh Routers (3)
- Modified OpenSPARC T1 Core
- MITTS (Traffic Shaper)
- L1.5 Cache
- CCX Arbiter
- FPU

To Other Tiles
System Overview

Tile
System Overview
System Overview
System Overview

Chip

Chipset

Chip Bridge

P-Mesh Off-Chip Routers (3)

P-Mesh Chipset Crossbars (3)
System Overview

Chip

Chipset

Chip Bridge

P-Mesh Off-Chip Routers (3)

P-Mesh Chipset Crossbars (3)

DRAM
System Overview

Chip Set

- Chip Bridge
- P-Mesh Off-Chip Routers (3)
- P-Mesh Chipset Crossbars (3)
- DRAM
- Wishbone SDHC
- AXI I/O
System Overview
Silicon Proven Designs: Piton

- 25-core
  - 2 Threads per core
  - Modified 64 bit OpenSPARC T1 Core
- 3 P-Mesh NoCs
  - 64 bit, 2D Mesh
  - Extend off-chip enabling multichip systems
- P-Mesh Directory-Based Cache System
  - 64kB L2 Cache per core (Shared)
  - 8kB L1.5 & L1 Data Caches
  - 16kB L1 Instruction Cache
- IBM 32nm SOI Process
  - 6mm x 6mm
  - 460 Million Transistors - Among largest chips built in academia
- Target: 1 GHz Clock @ 900 mV
- Received silicon and runs full-stack Debian in lab
OpenPiton+Ariane
OpenPiton+Ariane Cache Modifications

- New write-through cache subsystem with invalidations and the TRI interface
- LR/SC in L1.5 cache
- Fetch-and-op in L2 cache
OpenPiton+Ariane Platform Support

- Bootrom auto-generated with device tree from configuration
- RISC-V Debug
  - OpenOCD + GDB
  - Bootloading
- CLINT
- PLIC
  - lowRISC rv_plic
## Configurability Options

<table>
<thead>
<tr>
<th>Component</th>
<th>Configurability Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores (per chip)</td>
<td>Up to 65,536</td>
</tr>
<tr>
<td>Cores (per system)</td>
<td>Up to 500 million</td>
</tr>
<tr>
<td>Core Type</td>
<td>OpenSPARC T1</td>
</tr>
<tr>
<td></td>
<td>Ariane 64 bit RISC-V</td>
</tr>
<tr>
<td>Threads per Core</td>
<td>1/2/4</td>
</tr>
<tr>
<td>Floating-Point Unit</td>
<td>FP64, FP32</td>
</tr>
<tr>
<td></td>
<td>FP64, FP32, FP16, FP8, BFLOAT16</td>
</tr>
<tr>
<td>TLBs</td>
<td>8/16/32/64 entries</td>
</tr>
<tr>
<td></td>
<td>Number of entries (16 entries)</td>
</tr>
<tr>
<td>L1 I-Cache</td>
<td>Number of Sets, Ways (16kB, 4-way)</td>
</tr>
<tr>
<td>L1 D-Cache</td>
<td>Number of Sets, Ways (8kB, 4-way)</td>
</tr>
<tr>
<td>L1.5 Cache</td>
<td>Number of Sets, Ways (8kB, 4-way)</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>Number of Sets, Ways (64kB, 4-way)</td>
</tr>
<tr>
<td>Intra-chip Topologies</td>
<td>2D Mesh, Crossbar</td>
</tr>
<tr>
<td>Inter-chip Topologies</td>
<td>2D Mesh, 3D Mesh, Crossbar, Butterfly Network</td>
</tr>
<tr>
<td>Bootloading</td>
<td>SD/SDHC Card, UART, RISC-V JTAG Debug</td>
</tr>
</tbody>
</table>
FPGA Prototyping Platforms

Available:
• Digilent Genesys2
  • $999 ($600 academic)
  • 1-2 cores at 66MHz
• Xilinx VC707
  • $3500
  • 1-4 cores at 60MHz
• Digilent Nexys Video
  • $500 ($250 academic)
  • 1 core at 30MHz

In progress:
• Xilinx VCU118, BittWare XUPP3R
  • $7000-8000
  • >100MHz
• Amazon AWS F1
  • Rent by the hour
  • 1-N cores
  • Live demo at tomorrow's tutorial!
Roadmap

• Testing:
  • Memory consistency testing with litmus/herd/diy
  • Randomised testing with riscv-torture, RISC-V DV

• Bootloading:
  • OpenSBI
  • U-Boot/Coreboot/...

• Debian/Fedora Linux distro

• Performance enhancements
  • Multi-level TLBs
  • Branch Prediction improvements*
  • Increasing TRI/L1.5 line size
  • Multi-issue Ariane*

• Open backend flow for Ariane
• Tapeouts!

* GSoC project with FOSSi Foundation
Boot SMP Linux Today!

• Clone from:
  • [https://github.com/PrincetonUniversity/openpiton](https://github.com/PrincetonUniversity/openpiton)
  • Simulation with Modelsim, VCS, Verilator
  • FPGA implementation with Vivado 2018.2 or newer

• RV64GC Demo
  • 2 cores on Genesys2 at 66MHz
  • Play Tetris, browse the web!

• Tutorial tomorrow afternoon! (in this room)
  • Hands-on with Verilator simulation
  • Boot SMP Linux on FPGA
  • [http://openpiton.org/ISCA19_tutorial.html](http://openpiton.org/ISCA19_tutorial.html)
QUESTIONS?

@OpenPiton
http://openpiton.org

@pulp_platform
http://pulp-platform.org
### 2.5 Automatic Device Tree Generation

Table 3: Some of the supported FPGA build configurations

<table>
<thead>
<tr>
<th>Board Name / FPGA Type</th>
<th>Clock [MHz]</th>
<th>Config (X \times Y)</th>
<th>Core Type</th>
<th>FPU [y/n]</th>
<th>LUTs [k]</th>
<th>Registers [k]</th>
<th>RAM Tiles [#]</th>
<th>DSPs [#]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digilent NexysVideo</td>
<td>30</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>no</td>
<td>95 (71%)</td>
<td>72 (27%)</td>
<td>66 (18%)</td>
<td>16 (2%)</td>
</tr>
<tr>
<td>Artix 7</td>
<td>30</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>yes</td>
<td>110 (82%)</td>
<td>75 (28%)</td>
<td>66 (18%)</td>
<td>27 (4%)</td>
</tr>
<tr>
<td>7a200tsbg484</td>
<td>30</td>
<td>1 x 1</td>
<td>OpenSPARC T1</td>
<td>yes</td>
<td>115 (86%)</td>
<td>96 (36%)</td>
<td>59 (16%)</td>
<td>13 (2%)</td>
</tr>
<tr>
<td>Digilent Genesys2</td>
<td>67</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>no</td>
<td>86 (42%)</td>
<td>72 (17%)</td>
<td>66 (15%)</td>
<td>16 (2%)</td>
</tr>
<tr>
<td>Kintex 7</td>
<td>67</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>yes</td>
<td>99 (49%)</td>
<td>75 (18%)</td>
<td>66 (15%)</td>
<td>27 (3%)</td>
</tr>
<tr>
<td>7k325tffg900-2</td>
<td>67</td>
<td>1 x 1</td>
<td>OpenSPARC T1</td>
<td>yes</td>
<td>105 (52%)</td>
<td>91 (22%)</td>
<td>59 (13%)</td>
<td>16 (2%)</td>
</tr>
<tr>
<td></td>
<td>67</td>
<td>2 x 1</td>
<td>Ariane</td>
<td>no</td>
<td>141 (69%)</td>
<td>113 (28%)</td>
<td>124 (28%)</td>
<td>16 (4%)</td>
</tr>
<tr>
<td></td>
<td>67</td>
<td>2 x 1</td>
<td>OpenSPARC T1</td>
<td>yes</td>
<td>167 (82%)</td>
<td>120 (30%)</td>
<td>124 (28%)</td>
<td>54 (6%)</td>
</tr>
<tr>
<td></td>
<td>67</td>
<td>2 x 1</td>
<td>OpenSPARC T1†</td>
<td>yes</td>
<td>160 (79%)</td>
<td>137 (33%)</td>
<td>112 (25%)</td>
<td>32 (4%)</td>
</tr>
<tr>
<td>Xilinx VC707</td>
<td>60</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>no</td>
<td>99 (33%)</td>
<td>73 (12%)</td>
<td>63 (6%)</td>
<td>16 (&lt;1%)</td>
</tr>
<tr>
<td>Virtex 7</td>
<td>60</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>yes</td>
<td>114 (37%)</td>
<td>77 (13%)</td>
<td>63 (6%)</td>
<td>27 (1%)</td>
</tr>
<tr>
<td>7vx485tffg1761-2</td>
<td>60</td>
<td>1 x 1</td>
<td>OpenSPARC T1</td>
<td>yes</td>
<td>119 (39%)</td>
<td>97 (16%)</td>
<td>53 (5%)</td>
<td>16 (&lt;1%)</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>2 x 2</td>
<td>Ariane</td>
<td>no</td>
<td>284.1 (94%)</td>
<td>202 (33%)</td>
<td>237 (23%)</td>
<td>64 (2%)</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>3 x 1</td>
<td>Ariane</td>
<td>yes</td>
<td>268 (88%)</td>
<td>169 (28%)</td>
<td>179 (17%)</td>
<td>81 (3%)</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>3 x 1</td>
<td>OpenSPARC T1†</td>
<td>yes</td>
<td>255 (84%)</td>
<td>208 (34%)</td>
<td>158 (15%)</td>
<td>48 (2%)</td>
</tr>
<tr>
<td>Xilinx VCU118</td>
<td>100</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>no</td>
<td>90 (8%)</td>
<td>81 (3%)</td>
<td>88 (4%)</td>
<td>19 (&lt;1%)</td>
</tr>
<tr>
<td>Virtex US+</td>
<td>100</td>
<td>1 x 1</td>
<td>Ariane</td>
<td>yes</td>
<td>103 (9%)</td>
<td>84 (4%)</td>
<td>89 (4%)</td>
<td>30 (&lt;1%)</td>
</tr>
<tr>
<td>xcvu9pfpga2104-2L</td>
<td>100</td>
<td>1 x 1</td>
<td>OpenSPARC T1</td>
<td>yes</td>
<td>108 (9%)</td>
<td>100 (4%)</td>
<td>79 (4%)</td>
<td>19 (&lt;1%)</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>4 x 4</td>
<td>Ariane</td>
<td>no</td>
<td>923 (78%)</td>
<td>704 (30%)</td>
<td>963 (45%)</td>
<td>259 (4%)</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>4 x 2</td>
<td>Ariane</td>
<td>yes</td>
<td>583 (49%)</td>
<td>399 (17%)</td>
<td>495 (23%)</td>
<td>219 (3%)</td>
</tr>
</tbody>
</table>

† Without Coherence Domain Restriction [8] in caches.