Automating the Area-Delay Trade-off Problem

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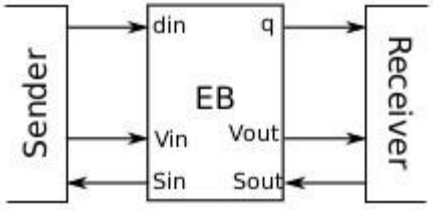
Area-Delay Trade-off Problem

- Fast clock speed
  - Many registers
  - More area/power usage
- Slow clock speed
  - Save on area/power with fewer registers
- Difficult to share code

Fluid Pipelines

- Type of latency insensitive (LI) system
- Fluid pipeline transformations
  - Add/remove registers
  - Change timing without changing behavior
  - No throughput loss
    - Lax ordering guarantee



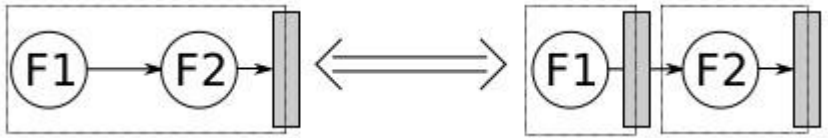
Elastic Buffer

Goal

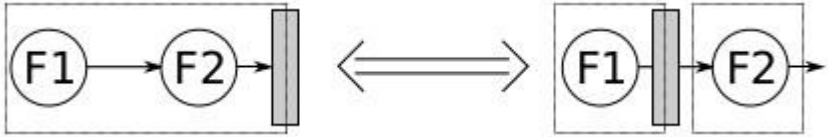
- Implement RISC-V architectures with Fluid Pipelines
- Investigate the viability of Fluid Pipeline transformations as a synthesis tool

Fluid Pipeline Transformations

- Correct by construction
  - No latency assumptions
  - Decouple behavior from timing
- Recycling and Retiming



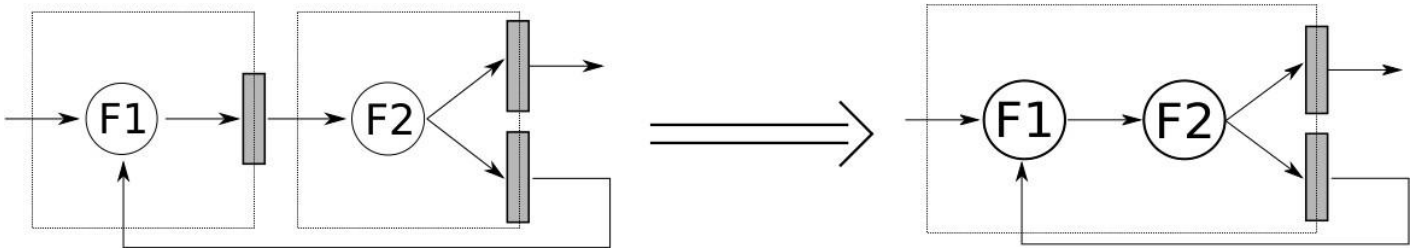
Recycling



Retiming

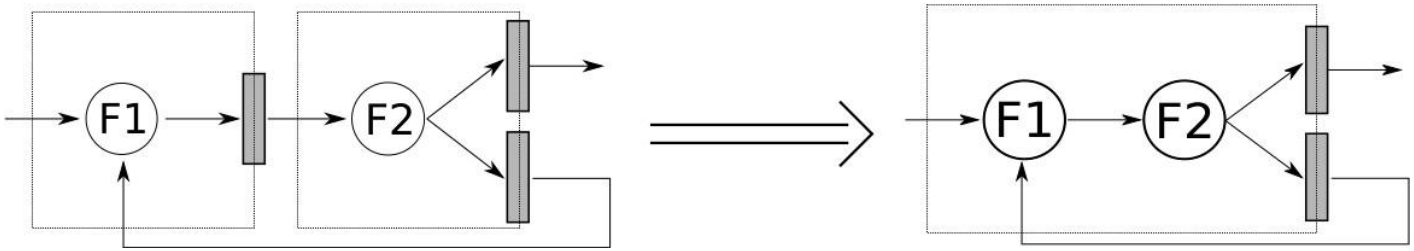
Fluid Pipeline Transformations

- *Merge* operation
  - Two stages of a pipeline: `merge(s1, s2)`
  - Forward and back connections
  - Not commutative: `merge(s1, s2) ≠ merge(s2, s1)`
    - Behavior is the same
    - Timing may be different



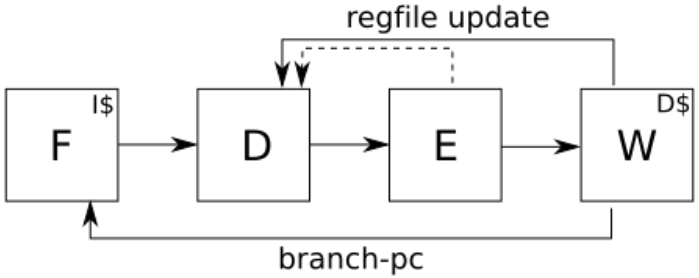
Fluid Pipeline Transformations

- Effect
  - Removes registers
  - CPI decreased
  - Potentially lengthen the critical path

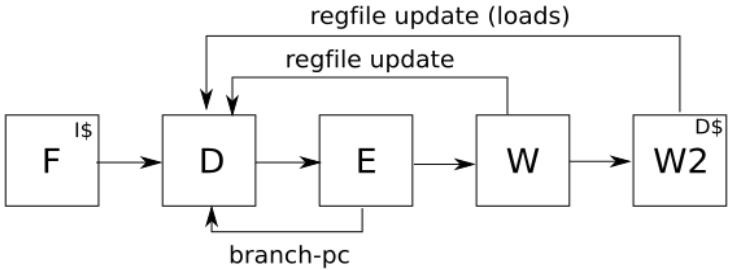


Cliff CPUs

- Four and five stage RISC-V 64i CPUs
  - c4 - 4-stage Cliff
  - c4+fwd - 4-stage Cliff with forwarding path (dotted line)
  - c5 - 5-stage Cliff



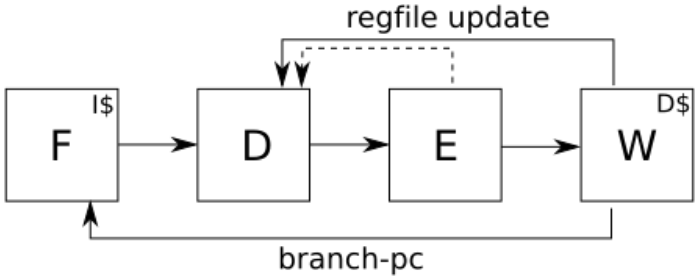
Cliff 4-stage



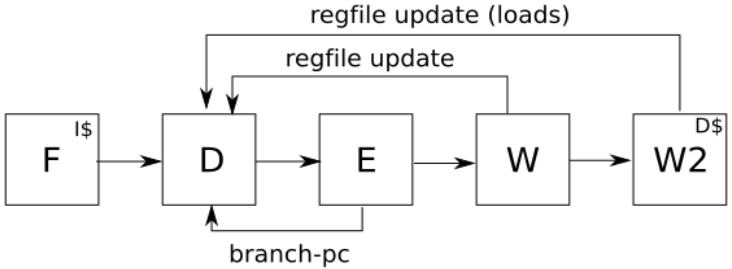
Cliff 5-stage

Cliff CPUs

- Transform to 2 and 3 stage cores
- Compare against others with similar features

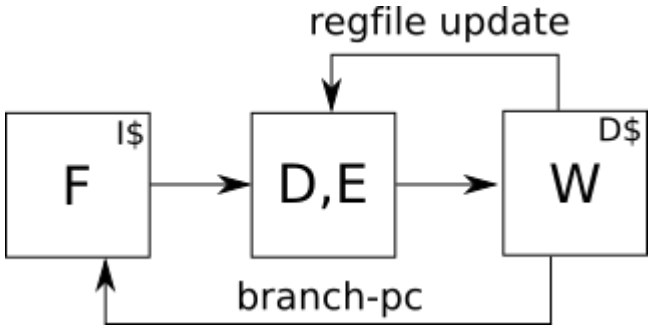


Cliff 4-stage

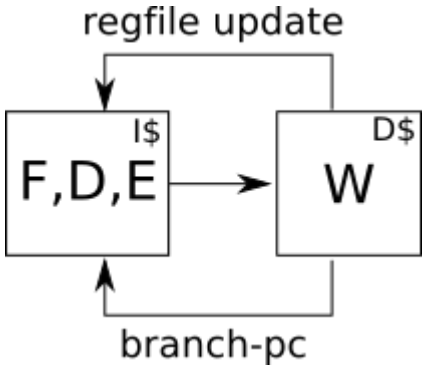


Cliff 5-stage

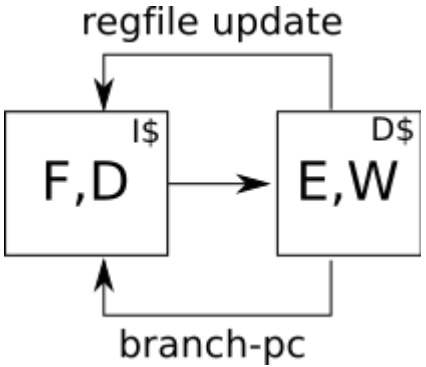
Cliff CPUs (Transforming)



Cliff 3-stage



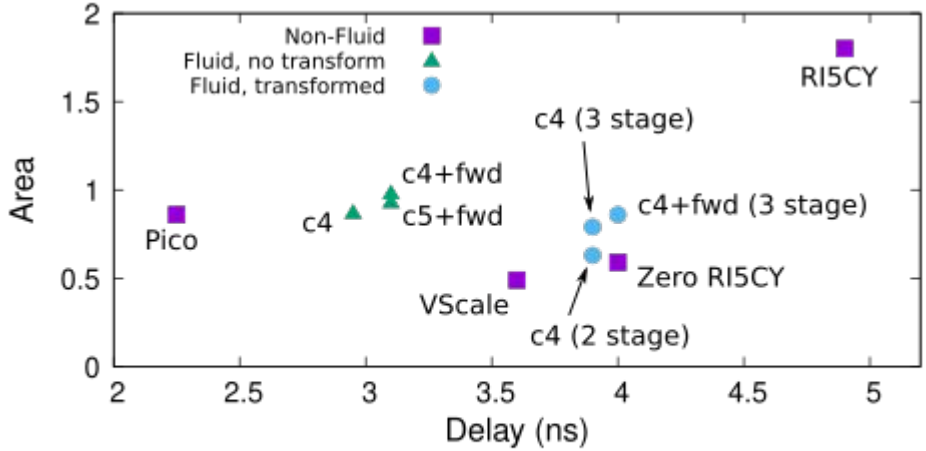
Cliff 2-stage



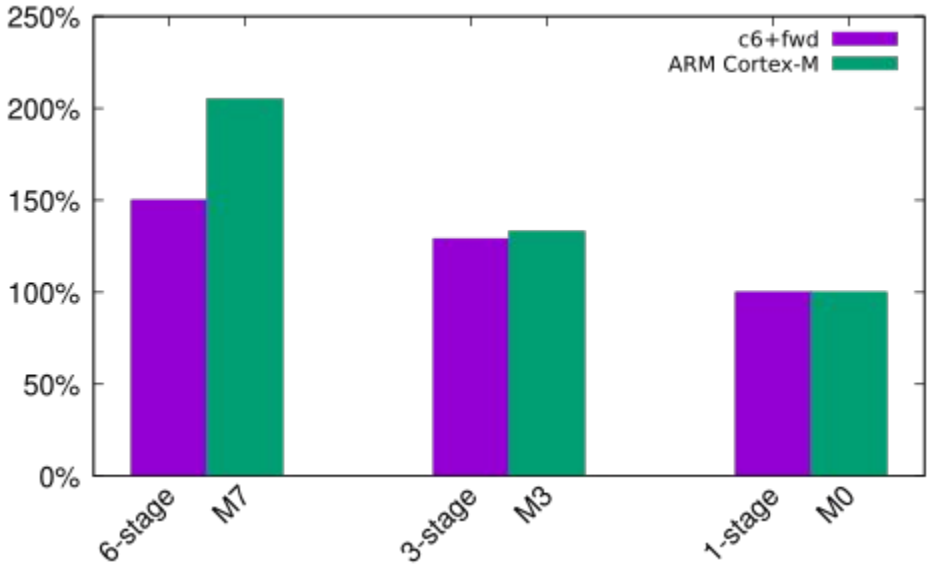
Cliff 2-stage (alt)

Evaluation

Area/Delay Pareto



Comparison to ARM Cortex-M



Conclusion

- Fluid pipeline transformations
  - Change timing while maintaining behavior
  - Code reuse
- So far only the `merge` operation
  - More transformations can allow for better tuning
  - Long term goal: frequency slide bar

Conclusion

- Other applications
  - Design space exploration
  - Fast simulation
  - SAT solver-based verification
- MASC Lab at UC Santa Cruz
  - Fluid pipeline based architecture toolchain
  - Leverage Transformations